Inventor Information for 10/783789

Inventor Name	City	State/Country
ZHENG, LEON	SAN JOSE	CALIFORNIA
LANGHAMMER, MARTIN	SOUTHWAY ALDERBURY	UNITED KINGDOM
PRASAD, NITIN	MILPITAS	CALIFORNIA
STARR, GREG	SAN JOSE	CALIFORNIA
HWANG, CHIAO KAI	FREMONT	CALIFORNIA
THARMALINGAM, KUMARA	SANTA CLARA	CALIFORNIA

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Inventor Name Search Result

Your Search was:

Last Name = ZHENG
First Name = LEON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10746448	Not Issued	71	12/24/2003	Programmable logic device with specialized functional block	ZHENG, LEON
10783789	Not Issued	71	02/20/2004	Flexible accumulator in digital signal processing circuitry	ZHENG, LEON
10783820	Not Issued	41	02/20/2004	Multiplier-accumulator block mode splitting	ZHENG, LEON
10783829	Not Issued	41	02/20/2004	Saturation and rounding in multiply-accumulate blocks	ZHENG, LEON
11488365	Not Issued	30	07/17/2006	Programmable logic device integrated circuit with dynamic phase alignment capabilities and shared phase-locked-loop circuitry	ZHENG, LEON
11670971	Not Issued	30	02/03/2007	Techniques For Compensating Delays In Clock Signals On Integrated Circuits	ZHENG, LEON
11737079	Not Issued	25	04/18/2007	Techniques For Reconfiguring Programmable Circuit Blocks	ZHENG, LEON
60790272	Not Issued	159	04/07/2006	Programmable logic device integrated circuit with dynamic phase alignment capabilities and shared phase-locked-loop circuitry	ZHENG, LEON

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ZHENG	LEON	Search

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Inventor Name Search Result

Your Search was:

Last Name = LANGHAMMER
First Name = MARTIN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09218974	6317771	150	12/22/1998	METHOD AND APPARATUS FOR PERFORMING DIGITAL DIVISION	LANGHAMMER, MARTIN
09511206	6400290	150	02/23/2000	NORMALIZATION IMPLEMENTATION FOR A LOGMAP DECODER	LANGHAMMER, MARTIN
09826527	6978287	150	04/04/2001	DSP PROCESSOR ARCHITECTURE WITH WRITE DATAPATH WORD CONDITIONING AND ANALYSIS	LANGHAMMER, MARTIN
09924354	6628140	150	08/07/2001	PROGRAMMABLE LOGIC DEVICES WITH FUNCTION-SPECIFIC BLOCKS	LANGHAMMER, MARTIN
09952223	6586966	150	09/13/2001	DATA LATCH WITH LOW-POWER BYPASS MODE	LANGHAMMER, MARTIN
09955645	6538470	150	09/18/2001	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	LANGHAMMER, MARTIN
09955647	6556044	150	09/18/2001	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	LANGHAMMER, MARTIN
09955654	6566906	150	09/18/2001	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	LANGHAMMER, MARTIN
09969977	Not Issued	161	10/02/2001	Programmable logic integrated circuit devices including dedicated hard-wired functional units and processor object components	LANGHAMMER, MARTIN
09975094	Not Issued	71	10/10/2001	Method and apparatus for protecting designs in SRAM-based programmable logic devices	LANGHAMMER, MARTIN
10032597	7035356	150	10/25/2001	EFFICIENT METHOD FOR TRACEBACK DECODING OF TRELLIS (VITERBI) CODES	LANGHAMMER, MARTIN
10132873	6781408	150	04/24/2002	PROGRAMMABLE LOGIC DEVICE WITH ROUTING CHANNELS	LANGHAMMER, MARTIN
10145322	7003544	150	05/14/2002	METHOD AND APPARATUS FOR GENERATING A SQUARED VALUE FOR A SIGNED BINARY NUMBER	LANGHAMMER, MARTIN

10212487	7173985	150	08/05/2002	METHOD AND APPARATUS FOR IMPLEMENTING A VITERBI DECODER	LANGHAMMER, MARTIN
10277627	6987401	150	10/22/2002	COMPARE, SELECT, SORT, AND MEDIAN-FILTER APPARATUS IN PROGRAMMABLE LOGIC DEVICES AND ASSOCIATED METHODS	LANGHAMMER, MARTIN
10331707	7260154	150	12/30/2002	METHOD AND APPARATUS FOR IMPLEMENTING A MULTIPLE CONSTRAINT LENGTH VITERBI DECODER	LANGHAMMER, MARTIN
10354440	6771094	150	01/28/2003	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	LANGHAMMER, MARTIN
10357749	7228531	150	02/03/2003	METHODS AND APPARATUS FOR OPTIMIZING A PROCESSOR CORE ON A PROGRAMMABLE CHIP	LANGHAMMER, MARTIN
10377962	6693455	150	02/26/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	LANGHAMMER, MARTIN
10384905	6714042	150	03/06/2003	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	LANGHAMMER, MARTIN
10437426	6958624	150	05/12/2003	DATA LATCH WITH LOW-POWER BYPASS MODE	LANGHAMMER, MARTIN
10625093	7024446	150	07/22/2003	CIRCUITRY FOR ARITHMETICALLY ACCUMULATING A SUCCESSION OF ARITHMETIC VALUES	LANGHAMMER, MARTIN
10660903	Not Issued	93	09/11/2003	ARRANGEMENT OF 3-INPUT LUT'S TO IMPLEMENT 4:2 COMPRESSORS FOR MULTIPLE OPERAND ARITHMETIC	LANGHAMMER, MARTIN
10678201	Not Issued	93	10/03/2003	MULTI-FUNCTIONAL DIGITAL SIGNAL PROCESSING CIRCUITRY	LANGHAMMER, MARTIN
10718968	Not Issued	41	11/21/2003	Logic cell supporting addition of three binary words	LANGHAMMER, MARTIN
10742746	7142010	150	12/19/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	LANGHAMMER, MARTIN
10746448	Not Issued	71	12/24/2003	Programmable logic device with specialized functional block	LANGHAMMER, MARTIN
10778930	6937062	150	02/12/2004	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	LANGHAMMER, MARTIN
10783789	Not Issued	71	02/20/2004	Flexible accumulator in digital signal processing circuitry	LANGHAMMER, MARTIN

10783820	Not Issued	41	02/20/2004	Multiplier-accumulator block mode splitting	LANGHAMMER, MARTIN
10783829	Not Issued	41	02/20/2004	Saturation and rounding in multiply-accumulate blocks	LANGHAMMER, MARTIN
10807796	Not Issued	41	03/23/2004	Digital signal processor	LANGHAMMER, MARTIN
10867456	7084664	150	06/14/2004	INTEGRATED CIRCUITS WITH REDUCED INTERCONNECT OVERHEAD	LANGHAMMER, MARTIN
10871868	7119576	150	06/18/2004	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	LANGHAMMER, MARTIN
10874790	7109753	150	06/22/2004	PROGRAMMABLE LOGIC DEVICE WITH ROUTING CHANNELS	LANGHAMMER, MARTIN
10932210	Not Issued	30	09/01/2004	Method and apparatus for implementing a look-ahead for low radix montgomery multiplication	LANGHAMMER, MARTIN
10938220	Not Issued	30	09/10/2004	Method and apparatus for protecting designs in SRAM-based programmable logic devices and the like	LANGHAMMER, MARTIN
10986428	Not Issued	30	11/10/2004	Mixed-mode multiplier using hard and soft logic circuitry	LANGHAMMER, MARTIN
11030801	7256715	150	01/07/2005	DATA COMPRESSION USING DUMMY CODES	LANGHAMMER, MARTIN
11042019	Not Issued	30	01/25/2005	FPGA configuration bitstream encryption using modified key	LANGHAMMER, MARTIN
11042032	Not Issued	30	01/25/2005	Encryption key obfuscation and storage	LANGHAMMER, MARTIN
11042477	Not Issued	30	01/25/2005	FPGA configuration bitstream protection using multiple keys	LANGHAMMER, MARTIN
11042937	Not Issued	30	01/25/2005	One-time programmable memories for key storage	LANGHAMMER, MARTIN
11049072	7109895	150	02/01/2005	HIGH PERFORMANCE LEMPEL ZIV COMPRESSION ARCHITECTURE	LANGHAMMER, MARTIN
11138895	Not Issued	160	05/25/2005	Specialized programmable logic region with low-power mode	LANGHAMMER, MARTIN
11145458	Not Issued	30	06/02/2005	Method and apparatus for limiting use of IP	LANGHAMMER, MARTIN
11151743	Not Issued	41	06/13/2005	Compare, select, sort, and median-filter apparatus in programmable logic devices and associated methods	LANGHAMMER, MARTIN
11155241	Not Issued	41	06/17/2005	Programmable logic integrated circuit devices including dedicated processor components and hard-wired functional units	LANGHAMMER, MARTIN
11201945	Not Issued	30	08/10/2005	DSP processor architecture with write Datapath word conditioning and analysis	LANGHAMMER, MARTIN

11208906	7230451	150	08/22/2005	PROGRAMMABLE LOGIC DEVICE WITH ROUTING CHANNELS	LANGHAMMER, MARTIN

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Your Search was:

Last Name = PRASAD
First Name = NITIN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09650790	6625796	150	08/30/2000	APPARATUS AND METHOD FOR PROGRAMMING A SET OF PROGRAMMABLE LOGIC DEVICES IN PARALLEL	PRASAD, NITIN
09703914	6400635	150	11/01/2000	MEMORY CIRCUITRY FOR PROGRAMMABLE LOGIC INTEGRATED CIRCUIT DEVICES	PRASAD, NITIN
09924354	6628140	150	08/07/2001	PROGRAMMABLE LOGIC DEVICES WITH FUNCTION-SPECIFIC BLOCKS	PRASAD, NITIN
10134886	6556502	150	04/26/2002	MEMORY CIRCUITRY FOR PROGRAMMABLE LOGIC INTEGRATED CIRCUIT DEVICES	PRASAD, NITIN
10269370	6707399	150	10/10/2002	DATA REALIGNMENT TECHNIQUES FOR SERIAL-TO-PARALLEL CONVERSION	PRASAD, NITIN
10315501	6981206	150	12/10/2002	METHOD AND APPARATUS FOR GENERATING PARITY VALUES	PRASAD, NITIN
10457874	Not Issued	41	06/10/2003	Apparatus and methods for communicating with programmable logic devices	PRASAD, NITIN
10458483	Not Issued	41	06/10/2003	Apparatus and methods for communicating information with programmable logic devices	PRASAD, NITIN
10625093	7024446	150	07/22/2003	CIRCUITRY FOR ARITHMETICALLY ACCUMULATING A SUCCESSION OF ARITHMETIC VALUES	PRASAD, NITIN
10769733	6911923	150	01/29/2004	DATA REALIGNMENT TECHNIQUES FOR SERIAL-TO-PARALLEL CONVERSION	PRASAD, NITIN
10783789	Not Issued	71	02/20/2004	Flexible accumulator in digital signal processing circuitry	PRASAD, NITIN
10783829	Not Issued	41	02/20/2004	Saturation and rounding in multiply-accumulate blocks	PRASAD, NITIN
11042477	Not Issued	30	01/25/2005	FPGA configuration bitstream protection using multiple keys	PRASAD, NITIN
11343919	Not Issued	30	01/30/2006	Programmable logic devices with function-specific blocks	PRASAD, NITIN
60189677	Not	159	03/15/2000	Quad-port memory	PRASAD, NITIN

	Issued				
60233389	Not Issued	159	09/18/2000	MULTIPLIER HARDCORE INCLUSION FOR PROGRAMMABLE LOGIC DEVICES	PRASAD, NITIN

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Your Search was:

Last Name = STARR
First Name = GREG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10137802	6633185	150	05/01/2002	PLL/DLL CIRCUITRY PROGRAMMABLE FOR HIGH BANDWIDTH AND LOW BANDWIDTH APPLICATIONS	STARR, GREG
10206415	6803803	150	07/26/2002	METHOD AND APPARATUS FOR COMPENSATING CIRCUITS FOR VARIATIONS IN TEMPERATURE SUPPLY AND PROCESS	STARR, GREG
10213115	6891401	150	08/05/2002	CLOCK LOSS DETECTION AND SWITCHOVER CIRCUIT	STARR, GREG
10353816	7159204	150	01/28/2003	SYSTEM AND METHOD FOR DESIGN ENTRY AND SYNTHESIS IN PROGRAMMABLE LOGIC DEVICES	STARR, GREG
10669295	6812756	150	09/23/2003	PLL/DLL CIRCUITRY PROGRAMMABLE FOR HIGH BANDWIDTH AND LOW BANDWIDTH APPLICATIONS	STARR, GREG
10761897	7064620	150	01/20/2004	SEQUENTIAL VCO PHASE OUTPUT ENABLING CIRCUIT	STARR, GREG
10783789	Not Issued	71	02/20/2004	Flexible accumulator in digital signal processing circuitry	STARR, GREG
10802590	6933869	150	03/17/2004	INTEGRATED CIRCUITS WITH TEMPERATURE-CHANGE AND THRESHOLD-VOLTAGE DRIFT COMPENSATION	STARR, GREG
10915201	7046048	150	08/09/2004	CLOCK LOSS DETECTION AND SWITCHOVER CIRCUIT	STARR, GREG
10921453	7023251	150	08/18/2004	PLL/DLL CIRCUITRY PROGRAMMABLE FOR HIGH BANDWIDTH AND LOW BANDWIDTH APPLICATIONS	STARR, GREG
10950190	Not Issued	160	09/23/2004	Process, temperature, and supply compensated delay circuit	STARR, GREG
11180311	Not Issued	160	07/12/2005	Sequential VCO phase output enabling circuit	STARR, GREG
11259156	Not Issued	61	10/25/2005	Sequential VCO phase output enabling circuit	STARR, GREG

11398384	Not Issued	41	04/04/2006	Clock loss detection and switchover circuit	STARR, GREG
11592734	Not Issued	17	11/03/2006	System and method for design entry and synthesis in programmable logic devices	STARR, GREG
60310135	Not Issued	159	08/03/2001	Process, temperature, and supply compensated delay circuit	STARR, GREG
60310136	Not Issued	159	08/03/2001	Clock loss detection circuit for switchover capability	STARR, GREG
60329896	Not Issued	159	10/16/2001	PLL/DLL architecture to support general and RF applications	STARR, GREG
60469541	Not Issued	159	05/09/2003	Sequential VCO phase output enabling circuit	STARR, GREG
11803530	Not Issued	17	05/14/2007	Preventing transistor damage	STARR, GREG W.
07832730	5174182	150	02/07/1992	MACHINE FOR FEEDING AND CUTTING SHEET MATERIAL	STARR, GREGORY
08121279	5408908	150	09/14/1993	CUTTING MACHINE	STARR, GREGORY
08888843	Not Issued	161	07/07/1997	DESK TOP MEASURING AND CUTTING MACHINE	STARR, GREGORY
09298548	6286403	150	04/22/1999	CUTTING MACHINE	STARR, GREGORY
09952223	6586966	150	09/13/2001	DATA LATCH WITH LOW-POWER BYPASS MODE	STARR, GREGORY
09955645	6538470	150	09/18/2001	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	STARR, GREGORY
09955647	6556044	150	09/18/2001	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	STARR, GREGORY
09955654	6566906	150	09/18/2001	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	STARR, GREGORY
10199339	Not Issued	161	07/19/2002	Stacking machine and method	STARR, GREGORY
10209633	6832173	150	07/30/2002	TESTING CIRCUIT AND METHOD FOR PHASE-LOCKED LOOP	STARR, GREGORY
10354440	6771094	150	01/28/2003	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	STARR, GREGORY
10377962	6693455	150	02/26/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	STARR, GREGORY
10384905	6714042	150	03/06/2003	SPECIALIZED PROGRAMMABLE	STARR, GREGORY

				LOGIC REGION WITH LOW-POWER MODE	
10393135	Not Issued	161	03/20/2003	Cover sheet applicator	STARR, GREGORY
10407632	7180334	150	04/03/2003	APPARATUS AND METHOD FOR DECREASING THE LOCK TIME OF A LOCK LOOP CIRCUIT	STARR, GREGORY
10437426	6958624	150	05/12/2003	DATA LATCH WITH LOW-POWER BYPASS MODE	STARR, GREGORY
10655853	7019570	150	09/05/2003	DUAL-GAIN LOOP CIRCUITRY FOR PROGRAMMABLE LOGIC DEVICE	STARR, GREGORY
10691152	6924678	150	10/21/2003	PROGRAMMABLE PHASE-LOCKED LOOP CIRCUITRY FOR PROGRAMMABLE LOGIC DEVICE	STARR, GREGORY
10742746	7142010	150	12/19/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	STARR, GREGORY
10746448	Not Issued	71	12/24/2003	Programmable logic device with specialized functional block	STARR, GREGORY
10778930	6937062	150	02/12/2004	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	STARR, GREGORY
10783820	Not Issued	41	02/20/2004	Multiplier-accumulator block mode splitting	STARR, GREGORY
10830562	7075365	150	04/22/2004	CONFIGURABLE CLOCK NETWORK FOR PROGRAMMABLE LOGIC DEVICE	STARR, GREGORY
10849319	Not Issued	30	05/18/2004	Dynamic phase alignment methods and apparatus	STARR, GREGORY
10871868	7119576	150	06/18/2004	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	STARR, GREGORY
11130079	7071743	150	05/16/2005	PROGRAMMABLE PHASE-LOCKED LOOP CIRCUITRY FOR PROGRAMMABLE LOGIC DEVICE	STARR, GREGORY
11135732	7193443	150	05/23/2005	DIFFERENTIAL OUTPUT BUFFER WITH SUPER SIZE	STARR, GREGORY
11138895	Not Issued	160	05/25/2005	Specialized programmable logic region with low-power mode	STARR, GREGORY
11256347	Not Issued	168	10/20/2005	Configurable clock network for programmable logic device	STARR, GREGORY
11282876	Not Issued	93	11/17/2005	CONFIGURABLE CLOCK NETWORK FOR PROGRAMMABLE LOGIC DEVICE	STARR, GREGORY

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Your Search was:

Last Name = HWANG
First Name = CHIAO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60225585	Not Issued	159	08/16/2000	SWITCH STRUCTURES FOR PROGRAMMABLE LOGIC DEVICE INTERCONNECT OR THE LIKE	HWANG, CHIAO K.
09931475	6661253	150	08/16/2001	PASSGATE STRUCTURES FOR USE IN LOW-VOLTAGE APPLICATIONS	HWANG, CHIAO KAI
09952223	6586966	150	09/13/2001	DATA LATCH WITH LOW-POWER BYPASS MODE	HWANG, CHIAO KAI
09955645	6538470	150	09/18/2001	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	HWANG, CHIAO KAI
09955647	6556044	150	09/18/2001	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	HWANG, CHIAO KAI
09955654	6566906	150	09/18/2001	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	HWANG, CHIAO KAI
10354440	6771094	150	01/28/2003	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	HWANG, CHIAO KAI
10377962	6693455	150	02/26/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	HWANG, CHIAO KAI
10384905	6714042	150	03/06/2003	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	HWANG, CHIAO KAI
10437426	6958624	150	05/12/2003	DATA LATCH WITH LOW-POWER BYPASS MODE	HWANG, CHIAO KAI
10637258	7119574	150	08/08/2003	PASSAGE STRUCTURES FOR USE IN LOW VOLTAGE APPLICATIONS	HWANG, CHIAO KAI
10742746	7142010	150	12/19/2003	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	HWANG, CHIAO KAI
10746448	Not	71	12/24/2003	Programmable logic device with	HWANG, CHIAO KAI

	Issued			specialized functional block	
10783789	Not Issued	71	02/20/2004	Flexible accumulator in digital signal processing circuitry	HWANG, CHIAO KAI
11138895	Not Issued	160	05/25/2005	Specialized programmable logic region with low-power mode	HWANG, CHIAO KAI
11319846	7216139	150	12/28/2005	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	HWANG, CHIAO KAI
11498214	Not Issued	30	08/01/2006	Passgate structures for use in low-voltage applications	HWANG, CHIAO KAI
10778930	6937062	150	02/12/2004	SPECIALIZED PROGRAMMABLE LOGIC REGION WITH LOW-POWER MODE	HWANG, CHIAO KAI
10871868	7119576	150	06/18/2004	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	HWANG, CHIAO KAI
11465252	Not Issued	71	08/17/2006	DEVICES AND METHODS WITH PROGRAMMABLE LOGIC AND DIGITAL SIGNAL PROCESSING REGIONS	HWANG, CHIAO KAI
11693520	Not Issued	19	03/29/2007	PROGRAMMABLE LOGIC DEVICE INCLUDING MULTIPLIERS AND CONFIGURATIONS THEREOF TO REDUCE RESOURCE UTILIZATION	HWANG, CHIAO KAI

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Your Search was:

Last Name = THARMALINGAM
First Name = KUMARA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10463688	7082592	150	06/16/2003	METHOD FOR PROGRAMMING PROGRAMMABLE LOGIC DEVICE HAVING SPECIALIZED FUNCTIONAL BLOCKS	THARMALINGAM, KUMARA
10783789	Not Issued	71	02/20/2004	Flexible accumulator in digital signal processing circuitry	THARMALINGAM, KUMARA
10783820	Not Issued	41	02/20/2004	Multiplier-accumulator block mode splitting	THARMALINGAM, KUMARA
11294702	Not Issued	30	12/05/2005	Method and apparatus for compiling programmable logic device configurations	THARMALINGAM, KUMARA
11550132	Not Issued	30	10/17/2006	CLOCK DISTRIBUTION FOR SPECIALIZED PROCESSING BLOCK IN PROGRAMMABLE LOGIC DEVICE	THARMALINGAM, KUMARA
11566982	Not Issued	25	12/05/2006	LARGE MULTIPLIER FOR PROGRAMMABLE LOGIC DEVICE	THARMALINGAM, KUMARA
11682787	Not Issued	25	03/06/2007	LARGE MULTIPLIER FOR PROGRAMMABLE LOGIC DEVICE	THARMALINGAM, KUMARA
60810765	Not Issued	159	06/02/2006	Flexible, area-efficient clocking methods for embedded DSP blocks	THARMALINGAM, KUMARA

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L2	3	1 and concatenat$3	US-PGPUB; USPAT	OR	ON	2007/08/07 14:38
L3	1	"6538470".pn.	US-PGPUB; USPAT	OR	ON	2007/08/07 14:39
L4	2	"20030141898"	US-PGPUB; USPAT	OR	ON	2007/08/07 14:39
L5	354	"708"/$.ccls. and @ad<"20040220" and concatenat$3 and (multiply$3 or multiplication or multiplier$1) and accumulat$3 and (add$3 or addition or subtract$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/07 14:46
L6	30	5 and (concatenat$3 with accumulat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/07 14:48
S1	2	"6538470".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 17:32
S2	3	"20030141898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 17:32
S3	34	("3473160" | "4871930" | "5122685" | "5128559" | "5371422" | "5483178" | "5689195" | "5754459" | "5825202" | "5874834" | "6069487" | "6078941" | "6154049" | "6215326" | "6255848" | "6404226").PN. OR ("6538470"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:49

EAST Search History

S4	15344	"708"/$.ccls. and @ad<"20040220"	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:50
S5	96	(zheng.in. and leon.in.) or (langhammer.in. and martin.in.) or (prasad.in. and nitin.in.) or (starr.in. and greg.in.) or (hwang.in. and chiao.in.) or (harmalingam.in. and kumara.in.)	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:52
S6	38	S5 and accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:52
S7	6	S6 and concatenat$3	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:56
S8	1	S6 and (concatenat$3.clm.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 17:55
S9	4367	S4 and accumulat$3	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:57
S10	3338	S9 and (multiplier$1 or multiplication or multiplying)	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:57
S11	340	concatenat$3 and S10	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 17:57
S12	119	S11 and programmable$1	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:36
S13	0	S12 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 17:58
S14	118	S12 and ("zero" or "0")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 17:58

EAST Search History

S15	58	S14 and initializ$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:01
S16	49	chat.xa. and accumulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:25
S17	73	chat.xa. and multiplier$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:25
S18	40	S17 not S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:25
S19	11	("4849922" | "5249146" | "5583803" | "5590066" | "5610849" | "5737256" | "5805482" | "6282555" | "6295320" | "6327602").PN. OR ("6732131").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:27
S20	21	("5053985" | "5181183" | "5249146" | "5345408" | "5452466" | "5574661" | "5610849" | "5636152" | "5671169" | "5724278" | "5825420" | "5986709" | "5995990" | "Re34734").PN. OR ("6295320"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:34
S21	365	"708"/$.ccls. and multiplier$1 and accumulat$3 and pixel$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:35

EAST Search History

S23	156	S21 and programmable$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:37
S24	32	("3872290" | "3980873" | "4718091" | "4720871" | "4747157" | "4791677" | "4937774" | "5005149" | "5027423").PN. OR ("5151953"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:41
S25	35	("3748451" | "4493048" | "4891689" | "4937774" | "5001663" | "5151953" | "5195050").PN. OR ("5311459").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:46
S26	1362	326/41.ccls. and @ad<"20040220"	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:47
S27	1448	326/41.ccls. and @ad<"20040220"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:46
S28	80	S27 and concatenat$3 and rout$3 and programmable$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:47
S29	3	S28 and accumulat$3 and (multiplier$1 or multiplication or multiplying)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 18:48
S30	27	("3473160" | "4871930" | "4912345" | "5122685" | "5128559" | "5371422" | "5483178" | "5689195" | "5744980" | "5754459" | "5825202" | "5874834" | "6069487" | "6215326" | "6362650" | "6407576" | "6453382" | "6467017" | "6538470" | "6556044" | "6628140").PN. OR ("6781408"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:49

EAST Search History

S31	58	("20020002574" | "20020041658" | "20030009659" | "20030028743" | "4777591" | "4777612" | "5043868" | "5258939" | "5282155" | "5297069" | "5297071" | "5311459" | "5343404" | "5428741" | "5500811" | "5502747" | "5517436" | "5532938" | "5588118" | "5590352" | "5613152" | "5642382" | "5680335" | "5710914" | "5748515" | "5764553" | "5787025" | "5787026" | "5790826" | "5839108" | "5867726" | "5896543" | "5904731" | "5926644" | "5941940" | "5987490" | "6058408" | "6078941" | "6092184" | "6119217" | "6167497" | "6175370" | "6175912" | "6230180" | "6230238" | "6230257" | "6247036" | "6260137" | "6266807" | "6292886" | "6321327" | "6327690" | "6349382" | "6425070" | "6496705" | "6510445" | "6532273" | "6532530").PN. OR ("7107302"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 18:51
S32	33	("4852035" | "5363408" | "5367476" | "5381357" | "5398073" | "5483529" | "5493343" | "5506636" | "5550596").PN. OR ("5642382"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/01 19:19
S33	515	multiplier$1 and programmable and "708"/$.ccls. and rout$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/01 19:20